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EXAMINER

STIGLIC, RYAN M

ART UNIT PAPER NUMBER

2112

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/759,819

Applicant(s)

HAYDEN, DOUGLAS TODD

Examiner

Ryan M. Stiglic

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 31-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 31-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-11 and 31-36 are pending and have been examined.
2. Claims 1-11 and 31-36 are rejected.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of claims 8, 34 and 36 describing connecting the SDA and SCL lines of figures 2-6 in a sequential order must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

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be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 8 is drawn to the connection order of power and reference (ground) contacts of a hot insertion device in which power is connected prior to the reference contact. Moreover the prior art teaches connecting the ground pin of a hot swap device prior to the connection of a power contact is industry standard and that connection in the reverse order will result in the destruction of logic devices as evidenced by Paul Li and his article titled "LVTC Logic family for live-insertion using standard CMOS process" (page 3). Applicant has not provided one of ordinary skill in the art with a disclosure of how to make the claimed invention contrary to the industry standard and without causing damage to the inserted device. In particular the specification (paragraph [0030] on page 7) merely states, "power line contact 62 makes contact with male side 58 before reference line contact 60" and does not meet the enablement requirement.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-6, 9-10, 31-33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh (US 5,729,062).

For claim 1 Satoh teaches:

A system comprising:

- a bus comprising signal lines (Fig. 5, items 15a and 15b; col. 4, ll. 38-50); and
- a device (Fig. 9, item 5) configured to be inserted onto and removed from the bus through contacts (Fig. 9, items 57-59) configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit (col. 5, line 62 – col. 6, line 27).

While Satoh discloses contacts configured to provide at different times during insertion and removal contact between a pre-charge circuit and a power supply line, and a low-impedance across the pre-charge circuit, Satoh does not expressly disclose such a pre-charge circuit and a low-impedance short circuit on the bus signal lines 15a and 15b of figure 5. Satoh however admits, “Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof (col. 7, ll. 1-3).”

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With regards to the teachings of Satoh, it is disclosed that implementing the invention of Satoh “...reduces the variation of the power source current to occur when the power source pin 19 of the package connector 18 is connected to the mother board connector and on the transition from the plug-in mode to the regular mode. Consequently, the package connector 18, mother board connector 24 and wirings are free from damage (col. 6, ll. 43-48).”

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the active plug-in circuit used to limit the in-rush current on the power supply line of figure 9 on the bus signal lines of figure 5 such that the in-rush current flow across the bus signal lines is reduced thus resulting in a device whose connector is free from damage.

The combination of figures 9 and 5 would thus result in the bus signal lines 18a and 18b being duplicated and appearing identical to the two signal lines on package connector 56 (Fig. 9) who mate with the current limiting circuit (resistor 50 of Fig. 9) and the low-impedance short circuit (the signal line connected to pin 57). Therefore the low-impedance short circuit and the current limiting circuit would be placed in series prior to the switches 15a and 15b since low-impedance short circuit and current limiting circuit are show in figure 9 to the first elements connected to the mother board connector 64.

For claim 2 Satoh teaches:

The system of claim 1, where the pre-charge circuit comprises a resistor located between one of the contacts and the device (Fig. 9, item 50; col. 6, ll. 18-20).

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For claim 3 Satoh teaches:

The system of claim 1, comprising a switch located between the contacts and the device (Fig. 5, items 15a and 15b; col. 4, ll. 38-50; the switches close only when the bus signal lines have been stabilized).

For claim 4 Satoh teaches:

The system of claim 3, where the switch is a field effect transistor located between the contacts and the device.

Satoh teaches that the switches (Fig. 5, 15a and 15b) are electronically controlled by the output of mode setting device 12 (Fig. 3) but does not explicitly state the switches are field effect transistors. Furthermore, Satoh admits knowledge of CMOS (Complimentary Metal Oxide Semiconductor) field effect transistors and their low power consumption (col. 4, ll. 51-57). As such *Official Notice* is taken that the use of field effect transistors as switching devices is well known to those skilled in the art.

For claim 5 Satoh teaches:

The system of claim 3, where the switch is configured to conduct after the low-impedance is provided across the pre-charge circuit (The switches 15a and 15b are closed only when the electronic circuit is stabilized as a result of the low impedance circuit [Fig. 9] connecting to the mother signal line [col. 4, ll. 38-50]).

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For claim 6 Satoh teaches:

The system of claim 1, comprising reference contacts configured to provide a common reference to the bus and the device before contact between the pre-charge circuit and one of the signal lines as the device is inserted onto the bus (Fig. 9, item 63).

For claim 9 Satoh teaches:

The system of claim 1, comprising power contacts, where the power contacts are configured to provide power at the same time as contact between, the pre-charge circuit and one of the signal lines, as the device is inserted onto the bus (Since the teachings of the power contacts is applied to the bus signal lines the power contacts and the bus signal contacts would thus connect at the same time).

For claim 10 Satoh teaches:

The system of claim 1, where the signal lines comprise a serial data line and a serial clock line (col. 4, ll. 38-50).

For claim 31 Satoh teaches:

A system, comprising:

- a bus comprising signal lines (Fig. 5, items 15a and 15b; col. 4, ll. 38-50);
- a device configured to be inserted onto and removed from the bus (Fig. 3, item 1) through contacts (Fig. 9, items 57-59) configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-

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impedance across the pre-charge circuit (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above),

- the contacts comprising a connector system including a first connector (Fig. 9, 57 as applied to line 18a or 18b of figure 5; please see rejection of claim 1 above), a second connector (Fig. 9, 59 as applied to line 18a or 18b of figure 5; please see rejection of claim 1 above), where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above).

For claim 32 Satoh teaches:

The system of claim 31 comprising:

- a third connector (Fig. 9, 57 as applied to line 18a or 18b of figure 5; please see rejection of claim 1 above); and
- a fourth connector (Fig. 9, 59 as applied to line 18a or 18b of figure 5; please see rejection of claim 1 above) where the third connector is configured to provide a second pre-charge circuit between the fourth connector and a second bus signal line, and the fourth connector is configured to provide a second short-circuit between the fourth connector and the second bus signal line, where the third connector and the fourth

connector are staggered to provide the second pre-charge circuit and the second short-circuit at different times during engagement and disengagement of the connector system (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above).

For claim 33 Satoh teaches:

The system of claim 32, where the first connector and the third connector are staggered to simultaneously provide the first pre-charge circuit between the second connector and the first bus signal line and the second pre-charge circuit between the fourth connector and the second bus signal line (Since the teachings of the power contacts is applied to both bus signal lines the connections associated with each bus signal would connect at the same time).

For claim 35 Satoh teaches:

The system of claim 33, where the second connector and the fourth connector are staggered to simultaneously provide the first short-circuit between the second connector and the first bus signal line, and the second short-circuit between the fourth connector and the second bus signal line (Since the teachings of the power contacts is applied to both bus signal lines the connections associated with each bus signal would connect at the same time).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh as applied to claim 1 above, and further in view of Paul Li.

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Satoh teaches a hot-insertion system (please see the rejection of claim 1 above) in which the power and reference lines connect at substantially equivalent times. Satoh does not expressly state implementing a staggered connection of power and reference lines.

Li teaches (page 3):

The major design guideline for hot-swap is that during hot-swapping, connect the ground pin of the inserting card to the ground pin of the motherboard before any other signal or power pins are connected. This is the main request for hot-swap. It is the industry standard for any hot-swap applications for both logic and switch devices. If the ground pins of the card and motherboard were not connected before any other pins during hot-swap, the voltage of the power and signal at connectors will go wild due to the lack of ground reference, and will burn the logic device designed for hot-swap.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to stagger the connection of the ground and power pins of Satoh such that voltages will not go wild due to lack of ground reference and will not burn the logic device.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh as applied to claim 1 above, and further in view of The I²C Specification.

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Satoh teaches the bus signal lines comprising a singular data line along with a clock signal much like an inter-integrated circuit (I²C) bus but does not explicitly state the two bus signal lines represent an I²C bus.

The I²C Specification teaches the I²C is an excellent choice for device communication because:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I2C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced (page 4)

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the data and signal line of Satoh as an I²C bus because the simple 2-wire serial I2C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks resulting in - smaller and less expensive PCBs.

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10. Claims 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh as applied to claim 1 above, and further in view of Liencres et al. (US 5,644,731).

Satoh teaches a hot insertion system (please see the rejection of claim 1 above) where the connection of a data signal line 18b (Fig. 5) and a clock signal line 18a (Fig. 5) occur at a substantially equivalent time. Satoh does not expressly teach that the connection of the clock and data signal lines can be staggered in a sequence.

Liencres teaches a hot insertion system similar to Satoh in that the connection of a plurality of bus signal lines (Fig. 3A, 3213a – 3213n; Fig. 4A, 4213a – 4213n) occur at a substantially equivalent time. In addition to this similar hot insertion system Liencres also teaches using convex and concave connectors (Fig. 5A and 5B) such that bus signal lines are connected in a staggered fashion. It is important to note however that the operations of the interfaces (both the simultaneous connection as shown in Fig. 3A and the staggered connections of Fig. 5A and 5B) are similar (col. 7, ll. 1-7) but the convex and concave connectors provide a shape that enhances immunity to a tilted insertion.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the convex or concave connector of Liencres into the hot-insertion system of Satoh such that the Plug-In package of Satoh is provided with staggered bus signal connections that enhance the immunity of a tilted card insertion.

Conclusion


11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure since it pertains to the hot-insertion of a device module.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMS


JOHN R. GOTTINGHAM
PRIMARY EXAMINER